REMARKS/ARGUMENTS

In the Office Action, the Examiner has objected to the drawings. We believe the description on page 9 is adequate for a proper understanding of the invention. However, we enclose a replacement sheet for Figure 2 including an arrow from the Data Recovery Unit 202 to the Frequency Control Unit 210.

In the Office Action, the Examiner has rejected claims 1-8 and 10-16 under 35 U.S.C. §103(a) as being unpatentable over Wang in view of U.S. Patent 6, 385,267 (hereinafter referred to as Bowen).

The Applicant respectfully submits that the subject matter claimed in claims 1-7 and 10-16, as amended, distinguishes patentably over the cited prior art references, as discussed below.

The Examiner's attention is directed towards the following limitations of claims 1. [***emphasis added***]:

Claim 1

1. A synchronizer for mapping an electrical digital signal of **arbitrary transmission rate for transport over a network** characterized by a range of allowable transmission rates, said synchronizer comprising:

   a) an input for receiving the electrical digital signal;

   b) a data recovery unit coupled to said input, said data recovery unit operative to recover from the electrical digital signal a stream of data bits and a first data clock signal indicative of the ***arbitrary transmission rate***;

   c) a clock generator unit coupled to said data recovery unit, said clock generator including a first input for receiving the first data clock signal and a second input for receiving a control signal, said clock generator unit being operative to multiply a frequency of the first data clock signal by a value indicated by the control signal for generating a second data clock signal, whereby **the second**

data clock signal is indicative of a line transmission rate that falls within the range of allowable transmission rates for the network;

d) a mapping unit in communication with said clock generator unit for receiving the second data clock signal, said mapping unit being operative for **mapping** the stream of data bits into at least one frame **at a line transmission rate indicated by the second data clock signal;**

e) an output for releasing the at least one frame from said synchronizer for transmission over the network.

The Applicant respectfully submits that Wang and Bowen, whether taken alone or in combination, do not disclose, teach nor suggest the invention claimed in claim 1. Without limiting the generality of the foregoing, neither reference teaches or suggests the highlighted portions of the claims. Without limiting the generality of the foregoing, neither reference teaches a system for mapping a signal having an **arbitrary transmission rate.**

The mapping of one rate or format into another is well known. Wang relates to removing waiting time jitter for know mappings. It does not teach how to map signals having arbitrary transmission rates. Accordingly, Wang does not teach or suggest the claimed invention, but rather suffers from the very problem discussed in the background section of the present application:

"Originally, optical transport networks were intended to be bit-rate and data format independent, thus providing for the transportation of a wide variety of data signals. Unfortunately, current optical transport networks, including SONET/SDH networks, do not achieve this goal, as the **line rates** for these networks have been **restricted to a set of discrete transmission rates**. Similarly, current electrical transport networks, such as the DS3 electrical network, are also limited to particular, discrete transmission rates. Thus, **data characterized by a transmission rate that does not belong to the set of pre-defined transmission rates is not directly transportable over such data networks**. In many cases, a user signal must undergo a mapping operation to be able to be transported by the data network.

The mapping of one rate or format into another is well known. For example, Bellcore TR-0253 describes in detail the standard mappings of the common

asynchronous transmission formats (DS0, DS1, DS2 and DS3, among others) into SONET. Similar mappings are defined for the ETSI hierarchy mapping into SDH.

Unfortunately, **the standards or proprietary schemes allow the transportation of only a very specific set of signals, with format specific hardware**. Thus, these methods of mapping **cannot** be used to **map rates that vary significantly from the standard**. Furthermore, these **mappings** are each **precisely tuned for a particular format and a particular bit-rate**, with for example a ±20ppm (parts per million of the bit rate) tolerance. If a signal has, for example, a bit rate even 1% different than that of a DS3, it cannot be transported over a SONET/SDH network. In addition, a different hardware unit is generally required to perform the mapping of each kind of signal." (emphasis added) (col 2, l 15-Column 3- line 13).

Neither reference discusses this problem or any solution to it.

Wang relates to multiplexing one or several lower rate signals into a higher rate signal in digital communication systems. The multiplexing of the lower rate signals can introduce a form of phase variation or jitter into the signals referred to as waiting time jitter. Wang relates to removing waiting time jitter from the signals. (Field of the Invention). It does address multiplexing plural lower rate signals into a higher rate signal, but it does this for conventional signals (i.e. for a set of discrete transmission rates). See background section generally, and in particular Column 2 lines 5-15, and Column 3, lines 8-10 wherein Wang describes the problem to be solved with reference to an example of a DS1 to DS2 mapping.

Accordingly, Wang does not teach the claimed invention in the way characterized by the rejection. The rejection appears to state that Wang teaches every element except for disclosing a clock generator performing frequency multiplication of the first clock on a first input and a control signal on a second input for generating a second clock. However, Wang also fails to teach at least elements b, c, and d of claim 1.

In any event, the rejection fails to establish a prima-facie case.

For the Patent Office to combine references in an obviousness analysis, the Patent Office must do two things. First, the Patent Office must articulate a motivation to combine the

references, and second, the Patent Office must support the articulated motivation with actual evidence. *In re Dembiczak*, 175 F.3d 994,999 (Fed. Cir. 1999). While the range of sources for the motivation is broad, the range of available sources does not diminish the requirement for actual evidence. *Id.* Once the Patent Office has properly combined the references, to establish *prima facie* obviousness, the Patent Office must still show where each and every claim element is shown. MPEP §2143.03.

The Bowen reference generally relates to the phase locking of signals, and more particularly relates to the phase alignment of video signals of arbitrary relative frequency. (Field of the invention). It is directed toward a system and method for phase aligning a first signal and a second signal, wherein the first and second signals have different frequencies. (Col 4, lines 13-16).

This is simply not directed to the problem solved by the present invention, nor does it teach or suggest a solution. It is not directed to a synchronizer for mapping an electrical digital signal of arbitrary transmission rate for transport over a network characterized by a range of allowable transmission rates. It makes no teaching or suggestions relating to mapping of signals of different rates let alone for transport over a network. It is not analogous at all to Applicants' instant invention.

Applicants respectfully submit that no proper motivation to combine exists, let alone has been established. Accordingly, the examiner's statement on page 4 of the rejection fails to establish the prerequisite requirements: "It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method and synchronizer of Wang by generating a second clock signal based on a frequency multiplication of a first clock signal and a control signal, as shown by Bowen. This modification provides a correlation between the first and second clock signals so that the integrity of the data can be maintained at the different clock rates while the use of such a control signal enables marginal increases and/or decreases in the generated clock when necessary.(Bowen; Col. 2, lines 55-57)" Neither this cited passage in Bowen or Bowen generally suggests modifying Wang to be able to map arbitrary rate signals.

Thus the rejection is improper for two reasons.

1) fails to establish a prima facie case:
   - as it fails to show any evidence for motivation to combine;
   - as the cited references are non analogous, from different fields, and offer different solutions to different problems, we submit that there is no reason to combine;
2) even if proper to combine (which is denied), the combination fails to teach each and every limitation.

Similar arguments apply for the remaining claims. Accordingly, withdrawal of the rejection and allowance of the application is solicited.

The Commissioner is hereby authorized to charge any additional fees, and credit any over payments to Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP.

Respectfully submitted,

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